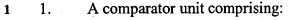
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- a first amplifier stage including a differential amplifier having a pair of input
- 3 nodes and a pair of output nodes, a switch connected across the pair of output nodes, and
- a non-linear load connected across the pair of output podes; and
- a second amplifier stage coupled to the pair of output nodes.
- 1 2. The comparator unit of claim 1, wherein the differential amplifier comprises a
- 2 pair of differential pairs of isolated gate field-effect transistors.
- 1 3. The comparator unit of claim 2, wherein the switch comprises an electronically
- 2 controllable switch.
- 1 4. The comparator unit of claim β , wherein the electronically controllable switch
- 2 comprises an isolated gate field-effect transistor.
- 1 5. The comparator unit of claim 4, wherein the non-linear load comprises a pair of
- 2 cross-coupled isolated gate field-effect transistors.
- 1 6. The comparator unit of claim 5, wherein each transistor in the pair of cross-
- 2 coupled isolated gate field-effect transistors comprises an n-channel isolated gate field-
- 3 effect transistor.
- 1 7. The comparator unit of claim 1, wherein the second amplifier stage comprises a
- 2 non-linear amplifier.
- 1 8. The comparator unit of claim 2, wherein the second amplifier stage includes a pair
- of second stage output nodes and a switch connected across the pair of second stage
- 3 output nodes.



- 1 9. The comparator unit of claim 1, wherein the differential amplifier comprises a
- 2 differential pair of isolated gate field-effect transistors.
- 1 10. A comparator unit comprising:
- a first amplifier stage including a differential amplifier having a pair of input
- nodes and a pair of output nodes including a first output node and a second output node, a
- 4 non-linear load connected across the pair of output nodes, and a first switch connected
- between the first output node and a common node and a second switch connected
- 6 between the second output node and the common node; and
- a second amplifier stage coupled to the pair of output nodes.

8

- 9 11. The comparator unit of claim 10, wherein the differential amplifier comprises a
- pair of differential pairs of isolated gate field-effect transistors.
- 1 12. The comparator unit of claim 11, wherein the switch comprises an optically
- 2 controllable switch.
- 1 13. The comparator unit of claim 12, wherein the optically controllable switch
- 2 comprises a photo-transistor.
- 1 14. The comparator unit of claim 13, wherein the non-linear load comprises a pair of
- 2 cross-coupled bipolar transistors.
- 1 15. The comparator unit of claim 14, wherein the second amplifier stage comprises a
- 2 non-linear amplifier
- 1 16. The comparator unit of claim 15, wherein the non-linear amplifier includes a pair
- of second stage output nodes and a switch connected across the pair of second stage
- 3 output nodes,

1	17.	The comparator unit of 16, wherein the non-linear amplifier includes a pair of
2	cross-c	oupled p-channel isolated gate field-effect transistors connected across the pair

second stage output nodes, a non-linear load connected across the pair of second stage

4 output nodes, and a pair of input transistors connected across the non-linear load.

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18. A signal transmission unit comprising:

a differential signal source;

a comparator unit comprising:

a first amplifier stage including a pair of differential amplifiers having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage coupled to the pair of output nodes; and a transmission line to couple the differential signal source to the comparator unit.

- 1 19. The signal transmission unit of claim 18, wherein the differential signal source is
- formed on a first integrated circuit die, the comparator unit is formed on a second
- integrated circuit die, and the transmission line is formed on a substrate on which the first
- 4 integrated circuit die and the second integrated circuit die are mounted.
- 1 20. The signal transmission unit of claim 19, wherein the second integrated circuit die
- 2 comprises a processor.
- 1 21. The signal transmission unit of claim 20, wherein the first integrated circuit die
- 2 comprises a communication unit.
- 1 22. The signal transmission unit of claim 20, wherein the first integrated circuit die
- 2 comprises a data storage unit.

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1	23.	The signal transmission unit of claim 20, wherein the first integrated circuit die	
2	comp	comprises an amplifier.	
1	24.	A method of processing a differential signal, the method comprising:	
2		beginning an equalization phase in a first amplifier stage;	
3		beginning an equalization phase in a second amplifier stage about one gate delay	
4	after beginning the equalization phase in the first amplifier stage;		
5		evaluating the differential signal in the first amplifier stage to form a first stage	
6	output differential signal after completing the equalization phase in the first amplifier		
7	stage; and		
8		evaluating the first stage output differential signal in the second amplifier stage	
9	after completing the equalization phase in the second amplifier stage.		
1	25.	The method of claim 24, wherein beginning an equalization phase in a first	
2	ampli	amplifier stage comprises:	
3		closing a switch in the first amplifier stage.	
1	26.	The method of claim 24, wherein beginning an equalization phase in a first	
2	amplifier stage comprises:		
3		closing a plurality of switches in the first amplifier stage.	
	•		
1	27.	The method of claim 26, wherein evaluating the differential signal in the first	
2	amplifier stage to form a first stage output differential signal after completing the		
3 .	equal	ization phase in the first amplifier stage comprises:	
4		applying linear amplification to the differential signal to form an amplified	
5 .	differ	differential signal; and	
6		applying non-linear amplification to the amplified differential signal to form the	
7	first s	tage output differential signal.	
	/		
1	28.	The method of claim 27, wherein evaluating the first stage output differential	

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signal in the second amplifier stage after completing the equalization phase in the second amplifier stage comprises:

applying non-linear amplification to the first stage output signal.

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